SPECIFICATION AMENDMENTS:

Please replace the paragraphs starting on page 4, line 7 through page 8, line 18 with the following amended paragraphs:

--In a multi-chip package 100, a first semiconductor chip (rectangular LSI chip in this case) 1 has a first face and a second face, on which first face a plurality of bonding pads 3-1 are arranged in such a manner as to go along four sides. Similarly, a second semiconductor chip (rectangular LSI chip in this case) 2 has a first face and a second face, on which first face a plurality of bonding pads 3-2 are arranged in such a manner as to go along four sides. The second semiconductor chip 2 is mounted in such a manner that its second face may face the first face of the first semiconductor chip 1. Each of the bonding pads 3-1 of the first semiconductor chip 1 and/or each of bonding pads 3-2 of the second semiconductor chip 2 is electrically connected with a lead 5 by using a wire 4 (part of which are only illustrated and they are not restrictive). In a certain case, the bonding pad 3-1 of the first semiconductor chip 1 and the bonding pad 3-2 of the second semiconductor chip 2 may be interconnected electrically. An auxiliary lead 6 supports the first semiconductor chip 1 at a corner of the first face of the first semiconductor chip and also extends out ~~of~~ from the first semiconductor chip 1. The plurality of auxiliary leads 6 are used to support the first face of the first semiconductor chip 1 with an adhesive agent ~~9~~ 8 (it is supported using an epoxy-based thermosetting adhesive material not shown in FIG. 1. It is not restrictive though).

Since the first face of the first semiconductor chip 1 is supported by the auxiliary leads 6, a thickness of a sealant 10 is determined by the respective heights of the first semiconductor chip 1, the second semiconductor ship 2, and the wire 4, so that the lead 6 has no influence on a total thickness of the sealant 10. Moreover, since the auxiliary leads 6 support the first semiconductor chip 1 at the corners of the first face of the first semiconductor chip 1 and also extend out ~~of~~ from the first semiconductor chip 1 (especially when the leads 5 are arranged so as to respectively face mutually opposite two sides of the first semiconductor chip 1), the wire 4 does not pass over the auxiliary lead 6 between the lead 5 and the bonding pad 3-1 or 3-2 at time of wire bonding. Further, since the auxiliary lead 6 supports the first semiconductor chip 1 at a given corner of the first face of the first semiconductor chip 1 and extends between extension lines of the first semiconductor chip 1 that sandwich the corner of the first face of the first semiconductor chip 1, it is possible to accommodate a shape that the leads 5 are arranged for every one of the four sides of the first semiconductor chip 1, thus making the present invention more applicable. In this case also, the wire 4 does not pass over the auxiliary lead 6 between the lead 5 and the bonding pad 3-1 or 3-2 at time of wire bonding. In particular, since the auxiliary lead 6 extends along a diagonal extension line of the first semiconductor chip 1, it is possible to accommodate a profile in which the lead 5 is arranged for every one of the four sides of the first semiconductor chip 1 and also to provide very high strength against twisting after sealing. Furthermore, by extending the auxiliary lead 6 along

the diagonal extension line of the first semiconductor chip 1, the lead 5 can be arranged in a large space, so that it is possible to bring the leads 5 close to the bonding pads 3-1 and 3-2 unlimitedly and also to reduce the height of the wire.

Furthermore, since the plurality of auxiliary leads 6 become gradually thick as ~~it extends~~ they extend toward an outside of the first semiconductor chip 1, stress applied on the first semiconductor chip 1 and the second semiconductor chip 2 when resin is poured can be made more even, thereby making the strength higher. Further, the auxiliary leads 6 are covered by an insulating protection film 7 (e.g., mixture of epoxy resin and poly-imide resin). By covering the auxiliary leads 6 by using th insulating protection film 7, the wire 4 can be prevented from coming in contact with the auxiliary lead 6 owing to pressure which is applied at time of sealing by use of the resin. It is, in turn, possible to prevent a yield from decreasing due to short-circuiting of the wire.

The first semiconductor chip 1, the second semiconductor chip 2, the bonding pads 3-1 and 3-2, the wires 4, the leads 5, the auxiliary leads 6, the insulating protection film 7, and the adhesive agent 9 are sealed by the sealant 10 (e.g., mold resin).

The following will describe a variant of the first embodiment. FIG. 3 is a top view of the variant of the multi-chip package according to the first embodiment of the present invention.

The variant of the first embodiment shown in FIG. 3 is different from the example shown in FIG. 1 in the shape of an auxiliary lead 26. The same

components of FIG. 3 as those of FIG. 1 are indicated by the same reference numerals and their detailed description is omitted. The auxiliary lead 26 of a multi-chip package 200 comprises at its tip a plurality of diverging portions 28. The ~~plurality of~~ diverging portions 28 are respectively arranged in the vicinity of each of the corners of a first face of a first semiconductor chip 21. Further, the diverging portions 28 each extend along a side of the first semiconductor chip 21. Furthermore, the auxiliary lead 26 and the diverging portions 28 of the auxiliary lead 26 are covered by an insulating protection film 27 (mixture of epoxy resin and poly-imide). The auxiliary lead 26 has the diverging portions 28 at its tip, so that it is possible to reserve a larger adhesion area. Of course, the diverging portions 28 are part of the auxiliary lead 26 and so support the first semiconductor chip 21 in ~~the~~ much the same way as the auxiliary lead 26. The area for adhering the first semiconductor chip 21 can thus be increased to increase strength with which the first semiconductor chip 21 is fixed, thereby preventing the first semiconductor chip 21 from being shifted due to pressure at time of sealing by use of the resin. Further, by arranging the auxiliary lead 26 along the side of the first semiconductor chip 21, it is possible to mount a larger second semiconductor chip 22 in a space surrounded by bonding pads 23-1 on the first face of the first semiconductor chip 21. Although part of the diverging portions 28 are arranged between the bonding pads 23-1 and leads 25, the diverging portions 28 are covered by the insulating protection film 27. Therefore, it is possible to prevent the wire 24 from coming in

contact with the auxiliary lead 26 and also the wire 24 from loosening and coming in contact with the auxiliary lead 26.--